Advance Technique in Demodulation of Non-Coherent Binary Phase Shift Keying

Ittee Teli
Electronics and Communication
G.B.P.Engg. College
Ghurdori Pauri Garhwal
Utrakhand, India

Abstract—Demodulation of Non Coherent Binary Phase Shift Keying, by using STEL -2110A Chip Circuity VDSP++4.5 software Technique, Both Time and Frequency recovery of the signal is possible, but in this paper only timing recovery process is discussed.

Keywords—Modulation; Demodulation; Binary Phase Shift Keying; Communication.

I. INTRODUCTION

The selection of the particular modulation method [1,5] used is determined by the application intended as well as by the channel characteristics such as bandwidth as susceptibility of the channel to fading. When radio communication in intended it must take account of antenna characteristics. When data transmission using a telephone channel is intended it take account of the fact that the channel may not transmit dc and low frequencies because of transformers which may be included in the transmission path. In each of these situations, a modulator at the transmitter and, at the receiver, a demodulator to recover the baseband signal. Such a modulator demodulator combination is called a MODEM. The Modulation techniques are of two types one is Analog and another one is Digital modulations. The Analog Modulation is as Amplitude, Frequency and Phase Modulation while Digital Modulation are Amplitude Shift Keying, Frequency Shift keying and Phase Shift Keying. Digital Modulations are of two type-coherent and non-coherent detection. Non coherent version is mostly used because off its less complexity. The coherent version of PSK is Binary Phase Shift Keying (BPSK) and non-coherent version is Differential Binary Phase Shift Keying (DPSK). The Binary Phase Shift Keying has some shortcomings, so Differential Binary Phase Shift Keying has been introduced. It is also known as the Differential Phase Shift Keying and it is modification of BPSK. The Demodulation of DPSK has been analyzed by STEL-2110A chip circuitry, which has Bit synchronizer/PSK Demodulator provides bit timing control the sampling of the signal in a receiver as well as a feedback signal to control the frequency of the local oscillator. It can be used in high speed coherent PSK, QPSK and DPSK modems in either continuous carrier or burst carrier (TDMA) environments.

II. NON COHERENT BINARY PHASE SHIFT KEYING

A. Modulation of Non Coherent PSK

As compare to digital modulation [2,6,7] Analog modulation is more sensitive to the noise present in the receiver so that digital modulation techniques are used instead of the analog modulation techniques. In the digital modulation techniques non-coherent is more used than coherent to reduce the complexity. Binary Phase Shift Keying (BPSK) is a type of phase modulation using 2 distinct carrier phases to signal ones and zeros. BPSK is the simplest form of PSK. It uses two phases which are separated by 180°.

If the sinusoid [10,11] is of amplitude ‘A’ it has a power Ps =1/2 A²

\[ d(t) = X-OR \]

\[ X-OR \rightarrow \) Balanced Modulator

\[ b(t-Tb) \]

\[ d(t) \]

\[ b(t) = +1V \] it is at logic level 0.

\[ b(t) = -1V \] it is at logic level 1.

Figure 1. Generation of Non coherent PSK

So that \( A = \sqrt{2}P_s \). Thus the transmitted signal is either

\[ V_{BPSK} = \sqrt{2}P_s \cos(\omega_0 t) \]

\[ V_{BPSK} = \sqrt{2}P_s \cos(\omega_0 t+\pi) \] or \( -\sqrt{2}P_s \cos(\omega_0 t) \)

In BPSK the data b(t) is a stream of binary digits with voltage levels which as a matter of convenience, it take to be at \(+1V\) and \(-1V\). When b(t) =1V it is at logic level 1 and when b(t) =-1V it is at logic level 0.

Hence,

\[ V_{BPSK}(t) = b(t) \sqrt{2}P_s \cos\omega_0 t \] (3)

In BPSK to regenerate the carrier, squaring b(t) \( \sqrt{2}P_s \cos\omega_0 t \). Accordingly, if the received signal were instead \(-b(t) \sqrt{2}P_s \cos\omega_0 t \), the recovered carrier would remain as before. Therefore it shall not be able to determine whether the received base band signal is the transmitted signal b(t) or \(-b(t) \). The carrier is generated by squaring the b(t) \( \sqrt{2}P_s \cos\omega_0 t \). Accordingly, if the received signal were instead \(-b(t) \sqrt{2}P_s \cos\omega_0 t \).
coso0,t, the recovered carrier would remain as before. Therefore it shall be unable to determine whether the received baseband signal is the transmitted signal Positive b (t) or negative b (t), it used the complicated circuitry to generate a local carrier at the receiver and at the demodulator for detecting a BPSK signal, synchronous carrier required.

To remove the all shortcoming of BPSK, DPSK is used.

<table>
<thead>
<tr>
<th>d(t)</th>
<th>b(t-Tb)</th>
<th>b(t)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>V</td>
<td>L</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>V</td>
<td>L</td>
<td>0</td>
</tr>
</tbody>
</table>

Where, L= Logic level, V=Voltage

The data stream to be transmitted d (t), is applied to one input of an exclusive -OR logic gate. To another gate input is applied the output of the exclusive or gate b (t) delayed by the time Tb allocate to one bit. This second input is then b (t-Tb).

Here it observe that, as required, b(t-Tb) is indeed b(t) delayed by one bit and it is given by:

\[ b(t) = d(t) \times (X-OR) b(t-Tb) \] (4)

By the observation of the response of b(t) to d(t) is that b(t) changes level at the beginning of each interval in which d(t) =1 and b(t) does not change level when d(t)=0. Thus in each successive bit interval b(t) changes from its value in the previous interval.

B. Demodulation of Non Coherent PSK

The recovery of the baseband signal is known as demodulation[7,11]. As is seen in Fig 1, b (t) is applied to a balanced modulator to which is also applied the carrier √ 2Ps cos ω0t. The modulator output, which is the transmitted signal is:

\[ V_{DPSK} (t) = b(t) \sqrt{2P_{s}} \cos(\omega_{0}t) \]

\[ = (b(t) \sqrt{2P_{s}} \cos \omega_{0}t) \] (5)

When d (t) =0 the phase of the carrier does not change at the beginning of the bit interval, while d (t) =1 there is a phase change of magnitude π.

A method of recovering the data bit stream from the DPSK signal is shown in Fig2. Here the received signal and received signal delayed by the bit time Tb are applied to a multiplier

\[ b(t) b(t-Tb) (2P_{s}) \cos (\omega_{0}t+\theta) \cos(\omega_{0}(t-Tb)+\theta) = b(t) b(t-Tb) \]

\[ P_{s} \{ \cos \omega_{0}T_{b} + \cos (2 \omega_{0} (T_{b}/2) +\theta) \} \]

(6)

The multiplier output is applied to a bit synchronizer and integrator for the BPSK demodulator.

\[ b(t) \sqrt{2P_{s}} \cos(\omega_{0}t+\theta) b(t-Tb) \sqrt{2P_{s}} \cos(\omega_{0}(t-Tb)+\theta) \] (7)

Figure 2. Demodulation of DPSK signal

The output integrator will suppress the double frequency term. It should select ω0Tb=+1 and the signal output will be large as possible. Further, with this selection the bit duration encompasses an integer number of clock cycles and the integral of the double frequency term is exactly zero. The transmitted data bit d (t) can readily be determine from the product b (t) b (t-Tb).

If d (t) =0 then there was no phase change and b (t) =b (t-Tb) both being -1V.

In this case b(t)b(t-Tb)=1. If however d(t)=1 then there was a phase change and either b(t)=1V with b(t-Tb)= -1V or vice versa. In either case b(t)b(t-Tb)=-1.

III. IMPLEMENTATION

The clock recovery portion [3,4,6]of the chip, is a digital phase locked loop which operates by integrating the input signals in the both the I and Q channels over one symbol period. This is done three times, in addition to the nominally “on time” integrations are also carried out. The difference between that last two gives an indication of signals. The signals can also be integrated prior to the main timing integrators. This can simplify operation over a wide range of data rates by maintaining a constant sampling rate, thereby eliminating the need to change the filter before the A/D converters. When the timing is correct then the averaged difference will be zero and this type of signals are used to drive a numerically controlled oscillator (NCO) which produces the clock signals to drive the entire circuit. Sampling of the incoming signals is controlled by the pre-accumulation control factor which is denoted by Ai. These pre-accumulation factors are the multiplication of two and it can be to one, two, four, eight or sixteen times. The optimally integrated IOPT and QOPT signals are used to drive a DPSK output and a feedback signal to control the local oscillator for carrier tracking. The signal can be selected to be phase locked loop (PLL) control signal or an automatic frequency control (AFC) signal. A PLL is essential a feedback control system. Which consists of 3 basic components and these components are Phase detector, low pass filter and voltage control oscillator. When the IOPT and QOPT signals will be the data outputs, and the latter is intended for use where fast acquisition is required, e.g., in burst carrier systems, such as Time Division multiplexing access TDMA, where the acquisition time of a PLL would case significant loss of a data at the beginning of each burst. In such case either differential demodulation should be used or a STEL-2110 Block Phase Estimation can be used to compensate for the residual phase roll in burst application. An output signal derived from I and Q data can be processed to give an indication of when the timing recovery circuit in lock.

A. Function Block Description

Following blocks are used to develop the logic of Demodulation of DPSK [3,4,10]

- I and Q Channel Integration Block
- Timing Discriminator Block
- Timing Generation Block
• Loop Filter Block
• Bit Timing NCO Block
• Lock Detector Block
• Carrier Discriminator Block

B. I and Q Channel Integration Block

The I and Q channel integrator block consists of two major sub-blocks: the pre-accumulators allow the signal to be integrated over 1 to 16 samples according to the setting of the pre-accumulation factor, Ai. Increasing the value of Ai gives a larger number of samples per symbol and allows the sampling rate to be maintained within a narrow range while the data rate varies over a wide range. The signal levels are automatically scaled and clipped to prevent overflow when a large number of samples are integrated in each symbol period. The outputs of the pre-accumulators are fed into the main I and Q channel integrators. In this section there are three accumulators in each channel for early, late and punctual integrations of the signals. The number of accumulations per symbol in this section can be either four or eight, so that number of input samples per symbol is the setting of control parameter multiplied with pre-accumulation factor.

C. Timing Discriminator Block

The difference between the Early and Late integration provide the discriminator function for the bit synchronizer function. The differential output from the I and Q channels are then summed and passed into the loop filter block. The individual I and Q channel components in the discriminator can also be disabled by means of the signal ICDD and QCDD. This allows the noise in these channels to be eliminated when receiving a BPSK signal once lock has been achieved. Demodulation is then coherent and the signal is all in one. The punctual integrations are then the optimal I and Q signal for each symbol. The combined discriminator signal is also available at pins BSD8-0.

D. Timing Generator Block

The timing generator block generates all the timing signals used internally from either numerically controlled oscillator NCO output or the ESCK signal. The input signal to the timing generator block is also the converter clock (CVCK) signal.

E. Loop Filter Block

The output of the timing discriminator block is normally passed into the loop filter block but a Multiplexer also allows other input signals to be used via the FBI8-0 inputs. The loop filter is effectively a second order filter since the accumulator of the bit-timing numerically controlled oscillator (NCO) is a part of the overall loop function, as shown in the diagram[3].

\[ H(z) = K(K1 + K2 \frac{z^{-1}}{1 - z^{-1}}) \]  

Where, the coefficients K1 and K2 are set by parameters stored in the programming registers and the values of K are system dependent. It is Z-transform based equation.

Figure 3. I and Q Channel Accumulator Block, Timing Discriminator Block, Timing Generator Block

F. Bit Timing Numerically Controlled Oscillator Block

The bit timing numerically controlled oscillator (NCO) derives the clock for the timing remaining parts, as well as for the sampling of the input signals, from the reference clock. The preset data is a 24-bit word (3bytes) and is loaded into the 24 MSBs of the 28-bit accumulator.

Figure 4. Loop Filter and Bit Timing NCO Block
The data from the loop filter block is added to this word so that the data from the loop filter modifies the 23 LSBs of the 28-bit phase accumulator derive the NCO. This allows the resolution of the 28-bit NCO to be maximized.

**G. Lock Detector Block**

The output of the timing discriminator block are combined to form a signal, which this signal is available on the lock outputs and an integrated version of it is available as the LI output. This magnitude of this signal is dependent on the lock acquisition. It can be compared to a threshold value to give lock indication.

![Lock Detector Block Diagram](image1)

In the lock detector block inputs are IOPT and QOPT, clock is AACK as a input for Lock Accumulation and output is through the lock accumulation.

**H. Carrier Discriminator Block**

The punctual I and Q signal from the I and Q channel integrator block are processed in the carrier discriminator. The dot and cross product of the I and Q signal are first formed.

Where,

\[
\text{Dot product} = I_n I_{n-1} + Q_n Q_{n-1}
\]

\[
\text{Cross product} = I_n Q_{n-1} - Q_n I_{n-1}
\]

![Non Coherent BPSK Demodulator I and Q Channel Processing](image2)

The dot product is brought out directly to be used for differential data in BPSK mode, and the cross product is also made available although it is not normally needed. Both are used to form the carrier discriminator function.

In the AFC mode this is:

- \(-\text{Sign (dot) } \times \text{cross}, \text{ for BPSK data}\)

In the PLL mode it is:

- \(-\text{Sign (I) } \times \text{Q, for BPSK data}\)

These functions are integrated under the control of the carrier accumulator clock (CACK) to form the discriminator output itself, which is available on the 16-bit CARD bus as well as via the microprocessor interface buffer.

**IV. VDSP++4.5 SOFTWARE**

Ith is an integrated development and debugging environment (IDDE) that provides complete graphical control of the edit, build, and debug processes[3,4].

Following are the Programming steps:

- C/C++ Compiler
- Assembler
- Linker
- Loader
- Simulation Software and code example

**A. Program Development Steps**

The following steps are required to program development

1. Create a project.
2. Configure project options.
3. Add and edit project source files.
4. Specify project build options.
5. Build a debug version (executable file) of the project.
6. Create a debug session and load the executable

**B. Features**

Visual DSP++ provides these features:

- It has Extensive editing capabilities. Create and modify source files by using multiple language syntax highlighting, drag and drops, bookmarks and other standard editing operations. View files generated by the code development tools.
- Flexible project management. Specify a project definition that identifies the files, dependencies, and tools that the build projects. Create this project definition once or modify it to meet changing development needs.
- Easy access to code development tools. Analog Devices provides these code development tools; C/C++ compiler, assembler, linker, splitter, and loader. Specify options for these tools by using dialog boxes instead of complicated command-line scripts. Options that control that the tools process inputs and generate outputs have a one-to-one correspondence to command-line switches. Define options for a single
file or for an entire project. Define these options once or modify them as necessary.

- Flexible project build options. Control builds at the file or project level. VisualDSP++ enables to build files or projects selectively, update project dependencies, or incrementally build only the files that have changed since the previous build. Views the statuses of project build in progress. If the build reports an error, double-click on the file name in the error message to open that source file. Then correct the error, rebuild the file or project, and start a debug session.
- VisualDSP++ Kernel (VDK) support. Add VDK support to a project to structure and scale application development. The Kernel page of the Project window enables to manipulate events, event bits, priorities, semaphores, and thread types.
- Flexible workspace management. Create up to ten workspaces and quickly switch between them. Assigning a different project to each workspace enables to build and debug multiple projects in a single session.
- Easy movements between debug and build activities. Start the debug session and move freely between editing, build, and debug activities.
- Easy-to-use debugging activities. Debug with one common, easy-to-use interface for all processor simulators and emulators, or hardware evaluation and development boards. Switch easily between these targets.

V. RESULT AND SIMULATION

The I and Q channel integrator in which Pre-accumulator and main accumulator are two blocks. The pre-accumulator allow the signal be integrated 12 samples according to the pre-accumulator factor as it increased then generates large number of sample per symbol and the sampling rate to be maintained within a narrow range while the data rate varies over the wide range. For to prevent the overflow, signal levels are automatically scaled and clipped.

The output of the pre-accumulator fed into the main I and Q channel integrators, these channel input is generated by the help of MATLAB. Where each channel has three accumulators for the early, late and on-time integrations. The number of accumulations per symbol in this section can be four or eight so it has been taken four accumulations per symbol, according to the setting of the control parameters, so that the total number of input samples per symbol is $S_s*A_i$.

Then, $12*2500=30,000$ total input samples per symbol

For the decision of early, late and on-time integration, It has been used that the signal is a rectangular pulse, which is synchronized to the input symbol timing.

The signal goes high one cycle of the signal which is generated by the numerical controlled oscillators (NCO) and is used extensively within the STEL-2110A. It is provided as an output to control the timing of A/D converters which precede the demodulator and the output of the A/D converters are sampled by the STEL-2110A on the rising edges of the signal before the beginning of these symbol period for one cycle of the converter clock i.e On-time. The signal is similar to On-time but goes high $\frac{1}{4}$ of a symbol period earlier i.e earlier integration and $\frac{1}{4}$ of a symbol period later ‘later integration’. It has been taken 12 element buffers; the process is done into the timing discriminator block. Where 12 element buffers are divided into the three group for the decision of early, late and on-time integration, in each group has four element. When the data reached from 0to3 position in the 12 element buffer i.e. early, form 4to7 is ‘on’ and 8to11 is late time integration Then the output of the timing discriminator loop fed into the loop filter loop, here the important work of the numerically controlled oscillator (NCO) to generate the clock for timing of the integration. The Bit-timing numerically controlled oscillator (NCO) derives the clock for the timing of the remaining parts of the system as well as for the sampling of the input signals, from the reference clock. It is part of the overall loop function, in the loop function $K_1$ and $K_2$ are coefficients these are set by parameters stored in the programming registers. For this, value of $K_1$ and $K_2$ are 8192 and 512 respectively. This provides the filtering in the loop filter block.

The output of the timing discriminator block are combined to form a signal which can be used to determine whether the system has acquired symbol lock or not this is done by the lock detector. Timing recovery is provided by early-late timing discriminator and by the loop-filter. The output of loop filter is added to the present value of NCO.

The output demodulated bit sequence is generated by taking the dot product of the output of ‘on’ time accumulator. The cross product is also provided in simulation program for frequency recovery. Phase Locked Loop (PLL) is used for the frequency recovery.

![Figure 7. Simulation of the input is generated by the MATLAB](image)

**Figure 7.** Simulation of the input is generated by the MATLAB
ACKNOWLEDGEMENT

Author is grateful to Dr. B.K.Kaushik G.B.P.E.C and Mr. L.C.Mangal Scientist ‘F’and Mr. Rajeev Shukla Scientist ‘c’ DRDO Dehradun for there valuable cooperation in the completion of the task.

REFERENCE


[4] ADSP-BF533 EZ-kit Lite Evaluation system, cross core Analog DSP++: chapter 5(Blackfin Hardware), Pg 1-16.


