ESD Protected Bandgap Reference Voltage Chip

S. Rama Devi
Department of ECE,
MVGR College of Engineering,
Visakhapatnam, A.P, India

D. Ramadevi
Department of ECE,
MVGR College of Engineering,
Visakhapatnam, A.P, India

Abstract—Bandgap Reference voltage chip is implemented in 0.25μm CMOS technology with ESD protection. This chip can be designed by using a layout tool micro wind 3.1.7 version. The chip circuit generates a reference voltage of 1.23 V. It can operate between 20ºC & 70ºC temperature. Band gap core produces a voltage that is insensitive to variation in temperature. It has a unique protection with respect to ESD and LATCHUP. The bandgap reference circuit is to design in CMOS process. This helps to avoid BICMOS process which is little bit complicated and much more expensive than CMOS process.

Keywords—Bandgap Reference; CMOS; BICMOS ESD; LATCHUP.

I. INTRODUCTION

A bandgap reference voltage chip is an essential component of analog to digital converter. It is often used to supply a reference voltage which is compared with other voltage.

Target: A fixed dc reference voltage that does not change with temperature.

As a well-established reference generator technique, bandgap reference is most popular for both Bipolar and CMOS technologies. The principle of the bandgap circuits relies on two groups of diode-connected BJT transistors running at different emitter current densities. By canceling the negative temperature dependence of the PN junctions in one group of transistors with the positive temperature dependence from a PTAT (proportional-to-absolute-temperature) circuit which includes the other group of transistors, a fixed DC voltage which doesn’t change with temperature is generated. This voltage is typically 1.23 volts, which is approximately the band gap of silicon.

II. ELECTROSTATIC DISCHARGE (ESD)

Proper handling precautions will minimize the risks of electrostatic discharge. ESD-sensitive components (including integrated circuits) should always be stored in static-shielded packaging. Grounded wrist straps and soldering irons can reduce potential opportunities for ESD discharges. Humidifiers, ionizers, and antistatic mats can minimize the buildup of static charges around workstations and machinery. These precautions reduce but do not eliminate ESD damage, so manufacturers routinely include special ESD protection structures on-board integrated circuits. These structures are designed to absorb and dissipate moderate levels of ESD energy without damage. Special tests can measure the vulnerability of an integrated circuit to ESD. The two most common test circuits are called the human body model and the machine model.

A. Human Body Model (HBM):

When the switch is pressed, a 150pF capacitor charged to a specified voltage discharges through the integrated circuit to ground. A 1.5k-Ω series resistor limits the peak current through the part. Ideally each pair of pins would be independently tested for ESD susceptibility, but most testing regimens only specify a limited number of pin combinations to reduce test time. Each pair of pins is subjected to a series of positive and negative pulses; for example, five positive and five negative. Modern integrated circuits are routinely expected to survive 2kV HBM. Specific pins on certain parts may be required to survive up to 25kV HBM.

B. Machine Model (MM):

A 200pF capacitor charged to a specified voltage discharges through the integrated circuit to ground. The test circuit contains no intentional series resistance, but practical testers incorporate some 20 to40 in wiring, switches, sockets, and so forth. This, together with the series inductance of the
wiring, limits the peak currents generated during testing. The machine model forms a much harsher test than the human body model; few parts can survive more than 500V under these conditions.

Figure 3. BGR block diagram with ESD protection PADs

Below the PAD circuits is used to protect the BGR circuit with out effecting ESD.

- GND ESD protection PAD
- SIGNAL ESD protection PAD
- SUPPLY ESD protection PAD

Figure 4. PAD circuits

III. CIRCUIT DESCRIPTION

A reference voltage is generated by adding two voltages that have temperature coefficients of opposite sign with suitable multiplication constants. The resulting voltage obtained is independent of temperature. The diode voltage drop across the base-emitter junction, VBE, of a Bipolar Junction Transistor (BJT) changes Complementary to Absolute Temperature (CTAT). Whereas if two BJTs operate with unequal current densities, then the difference in the base emitter voltages, ΔVBE, of the transistors is found to be Proportional to Absolute Temperature (PTAT). The PTAT relationship is given by,

\[ \Delta V_{BE} = V_T \ln m; \quad V_T = kT / q \]

Where, \( k \) is Boltzmann’s constant, \( T \) is the absolute temperature, \( q \) is the electron charge and \( m \) is the ratio of the current densities of the two BJTs. The PTAT voltage may be added to the CTAT voltage with suitable weighting constants to obtain a constant reference voltage.

Figure 5. Block diagram of Bandgap Reference Circuit
Fig. 5 shows the block diagram of the bandgap reference circuit designed. By using a supply independent current source, a current ISS is passed through BJT A. The same current ISS flows through m transistors connected in parallel, identical to A. Thus the current density of A is m times the current density of the m BJTs identical to A, connected in parallel. The voltages at node X and Y are maintained at the same value, VBE using a feedback network through a differential amplifier. This results in a voltage of ΔVBE, across the resistor R. The voltages VBE and ΔVBE are added to obtain the reference voltage. The circuit also requires a startup circuit since there exists a stable state at which no current flows through the circuit. The startup circuit forces the transistors to turn on and the circuit to operate at its other stable state to generate the reference voltage.

\[ V_{ref} = V_{BE} + \Delta V_{BE} \cdot \frac{R_1}{R_2} \]

R2 is the weighting constant. Thus by selecting the value of R2 the weighting constant may be set. This arrangement provided an elegant arrangement to generate the reference voltage while conserving voltage headroom. The circuit has a stable operating point at which no current to flows through it. An arrangement must be made to force the saturation when the supply is turned on. This function is carried out by the startup circuit. Thus output voltage is actually summation of a positive TC and a negative TC voltage. By choosing the proper value of resistors, output reference voltage is made constant with respect to temperatures (Zero TC).

\[ V_{BE} + M \frac{kT}{q} = V_{CG0} \frac{kT}{q} \ln \left( \frac{I_o}{I_C} \right) + M \frac{kT}{q} \]

Combining VBE and an appropriately scaled version of KT/q produces a temperature independent voltage, equal to VG0.

Figure 6. Voltage Temperature Plot

Figure 7. Band gap reference circuit with CMOS

IV. ANALOG LAYOUT

A. Resistors
- Dummy resistor should be added in order to minimize the faster etching in large areas
- In order to minimize the noise, the resistor can be designed
1) with a guard ring
2) inside a well to reduce the coupling to the substrate.

B. Fingering
- Analog transistor often having large W/L Use identical finger geometries.
- Transistors of different widths and lengths match very poorly. Even minimally matched devices must have identical channel lengths Most matched transistors require relatively large widths and are usually divided into sections, or fingers.
- Each of these fingers should have the same width and length as all others.
1) Inter-digitized
Matching obtained by dividing the gates in two

![Diagram of inter-digitized matching](image1)

Figure 9. Inter-digitized

2) Common-centroid
Common-Centroid layout design guidelines:

a) Placement: The geometric center of the devices to match must be very near.

b) Symmetry: The layout of the devices must be evenly distributed in both directions: x and y.

c) Regularity: Partial devices must be distributed uniformly.

d) Dispersion: The layout must be as compact and square as possible.

e) Orientation: The number of partial devices oriented in each direction must be the same for each device to be match

![Diagram of common-centroid layout](image2)

Figure 10. Common-Centroid

V. MICROWIND3

The MICROWIND3 program allows the student to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND3 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, Verilog compiler, tutorial on MOS devices). You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

VI. ANALYSIS OF SIMULATION RESULTS

A. Variation of reference voltage with respect to temperature:

It can be seen from the wave shape, reference voltage is approximately 1.2 V at room temperature. Reference voltage varies very little from 0 to 100 and remain almost constant from 20 to 70. Total variation of reference voltages is about 2.6 mV which is 0.213% of reference voltage. This same variation is 0.63% of reference voltage when the bandgap reference circuit designed with a single stage amplifier.

![Graph of reference voltage variation with temperature](image3)

Figure 12. Variation of reference voltage with respect to temperature
B. Variation of reference voltage with respect to $V_{DD}$

![Graph showing variation of reference voltage with respect to VDD](image)

AS supply voltage $V_{DD}$ changes from 3V to 7V, the changes in reference voltage is about 11mv, which is 0.27% with respect change in VDD. This same reference voltage is 0.35% with respect to change in VDD, when band gap reference circuit is designed with single stage amplifier.

VII. CONCLUSION

A bandgap reference with a current feedback mode has been designed. The circuit uses no external current sources and is designed to have a zero temperature coefficient at 27°C. The design is implemented with 0.25 μm CMOS process and consumes very little headroom. The chip occupies a total area of the chip has been optimized by combining all the MOSs. Most of the area is taken up by the pnp transistors, so it cannot be optimized too much. The bandgap reference circuit can support a zero current even when the power supply is on. So for proper operation the circuit needs to be turned on. This helps to avoid BiCMOS process.

REFERENCES